

T7 DPU Products

High Performance Programmable DPU 1/10/25/40/50/100/200/400GbE Controller

Enables several offloads, programmable compute, encryption, FPGA integration, virtualization over a single wire.

Highlights

- Full suite of Storge features
- Full suite of Cloud features
- Full suite of data center networking features
- Full suite of data streaming features
- Full suite of encryption functions
- Embedded programmable DPU
- Embedded Arm A72 cores, accessible by user
- Adapter or micro-server functionality
- Ability to integrate with an external FPGA
- Integrated Ethernet and PCIe switch
- Software Compatible with T4, T5, and T6

Applications

Datacenter Networking

- Scale out servers and NAS systems
- Consolidate LAN, SAN, and cluster networks (run InfiniBand and Fibre Channel applications on Ethernet)
- Enhanced network and server security

Cloud Computing

- Virtualization features to maximize cloud scaling and utilization
- Cloud-ready functional and management features
- Secure Sockets offload
- Full support for overlay products
- Seamless integration with external FPGA

Networked Storage

- Develop high-performance shared-storage systems providing both file and block level services
- Computational Storage
- Ethernet to the Drive
- Integrated encryption support
- NVMe Fabrics (iWARP & RoCEv2)
- NVMe/TCP (including NVMe offload)
- Very high data-integrity
- Dedupe, Compression support
- RAID, Erasure Coding support

High Performance Computing

- Very low latency Ethernet
- High performance RDMA support
- Increase cluster fabric bandwidth

Streaming Applications

- Internet attack protection
- QoS and Traffic Management
- Video streaming

Edge Products

- Micro ServersGateways
- 5G Appliances
- Firewalls

Overview

Chelsio's T7 is a quad port 1/10/25/50/100Gb, dual port 40/100/200Gb, or single port 400Gb Ethernet Unified Wire DPU ASIC with a PCI Express 5.0 host bus interface, optimized for storage, cloud computing, HPC, virtualization and other datacenter networking applications.

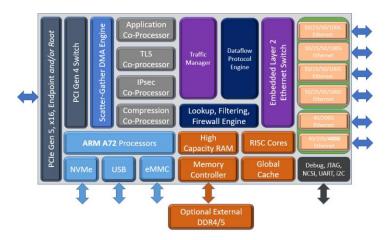
The seventh generation T7 ASIC technology from Chelsio provides the highest performance and efficiency, with dramatically lower host-system CPU communications overhead thanks to on-board hardware that offloads TCP/IP, UDP/IP, iSCSI, FCoE, Unified RDMA (RoCEv2 & iWARP), TLS/IPsec, NVMe-oF, and NVMe/TCP processing from its host system and frees up host CPU cycles for user applications. As a result, the system benefits from higher bandwidth, lower latency, and reduced power consumption.

T7 runs the predecessor T4, T5, & T6 silicon software without modification so as to enable leveraging of the user's existing software investment.

T7's architecture is Chelsio's 7th generation DPU technology road-tested across several tier-1 OEMs over the years and has evolved to support all offloads using either card memory or host memory. As a result, T7 technology can now enable a full featured DPU technology in a small memory-free package to address server and cloud applications at an aggressive price point.

The Smart NIC Programmable DPU Solution

In addition to the above offloads, versions of T7 integrate 8 A72 Arm cores that are exposed to the user. These Arm cores offload the traffic to the integrated 400Gb DPU on the chip and as a result the Arm cores are available to support the user's specific application. The T7 transport engine is a programmable DPU that can offload protocol processing per connection, per-server, per-interface, while simultaneously providing complete stateless offload to traffic for non-offloaded connections (processed by operating systems stack running on host CPU). The T7 also provides a flexible direct data placement capability for regular TCP sockets, with all the benefits of zero-copy and kernel bypass without rewriting the applications. To support the Arm Cores, Chelsio provides a full development and debug software package to allow development of application specific firmware.



T7 Block Diagram

Features

	T7	N7		T7	N7		T7	N7
Host Interface			Storage			TCP & UDP Offload		
PCI Express Gen5 x16	~	~	iSCSI initiator and target mode stack	~	~	Full TCP stack including IPv4 & IPv6	•	~
Integrated PCIe switch	~		Full FCoE offload (Initiator or Target)	~	~	Extensive RFC compliance, fully featured	~	~
Integrated PCIe bridge	~		Open FCoE offload (Initiator)	~	~	VLAN support up to 4096 VLAN IDs	~	~
End Point or Root Complex operation	~		T10 DIF/DIX support for iSCSI	~	~	Load balancing and failover capabilities	~	•
MSI-X, MSI, legacy pin interrupts	~	~	NVMe-oF Offload (iWARP or RoCEv2)	~	~	UDP Sockets API	•	•
			NVMe/TCP Offload	~	~	Low user-to-user latency	~	•
Wire Interface			QUIC Offload	~	~	Multicast replication on ingress or egress	•	•
2x1/10/25/40/50/100G	~	~	Dedupe offload	~		Patented Seamless Failover	~	~
4x1/10/25/50/100G	~	~	Erasure Code offload	~		Proxy Switching	•	~
2x40/100/200G	~	•	RAID 5/6 offload	~		High capacity offload without card memory	~	~
1x400G	~	~	Compression (LZ77+Huffman, Gzip, XP10, zlib)	~				
56Gb PAM4, or 25Gb NRZ	~	~	PMoF	~		High Performance RDMA		
IEEE 802.3bj (100 GbE over copper/backplane)	~	~	iSER	~	~	Native RoCEv2 support	•	~
IEEE 802.3cd (50/100/200 GbE)	~	~	Data-at-rest encryption	~	~	Native iWARP support	~	~
IEEE 802.3ba (40/100 GbE)	~	~				All to All support	~	~
IEEE 802.3ae (10 GbE)	~	~	Security					
IEEE 802.3az Energy Efficient Ethernet	~	~	AES 128/256 and SHA1/SHA2 offload	~	~	Data Center Features		
IEEE 802.3z (1GbE)	~	~	TLS and IPsec support	~	~	Internet Attack Protection	~	~
IEEE 802.1p Priority	~	~	Inline & co-processor modes	~	~	PFC, DCB, CEE	~	~
IEEE 802.1Q VLAN Tagging	~	~	SM2, RSA, ECC, ECDH, ECDSA, DSA, DH	~		Time stamping support	~	~
IEEE 802.1Qbg EVB/VEPA	•	~	Inline IPsec & TLS for all Offload Traffic	~	•			
IEEE 802.1BR Bridge Port Extension	~	~	Integrated Block or inline encryption	~	~	Embedded Processors		
IEEE 802.1Qau Congestion Notification	•	~	True Random Number Generator	~	•	ARM A72 Cores, 2MB L2 Cache	8	
IEEE 802.3x Flow Control	~	~	Secure firmware update	~	~	RISC Cores	8	8
IEEE 802.3ad Load-balancing and Failover	•	~	Hardware Root of Trust support	~	•	400Gb DPU Core	1	1
Ethernet II and 802.3 encapsulated frames	~	~				Dual-Channel 4800MT/s DDR5 8GB	~	V
Multiple MAC addresses per interface	~	~	Cloud & Virtualization					
Jumbo Frames up to 9.6 Kbytes	~	~	NVMe Virtualization/Emulation	~		Management and Other Interfaces		
ITU-T G.8262, Sync-E	~	~	Virt-IO	~		USB 2.0 Host Mode	•	
			OVS Offload	~		UART	~	~
Stateless Offloads			Seamless integration with external FPGA	~		eMMC 4.51	~	
TCP/UDP checksum offload for IPv4 & IPv6	~	~	Inband Telemetry	~	~	NVMe Gen 4, x2	~	
TSO, LSO, and GSO for IPv4 & IPv6	~	~	NVGRE, VXLAN and GENEVE support	~	~	NC-SI	~	~
VLAN filtering, insertion & extraction	~	~	PCI-SIG SR-IOV, 256 VF, 8 PF	~	~	SPI Flash	~	~
Packet filtering and attack protection	~	•	264 port virtual switch	~	~	I2C, MDIO, GPIO, JTAG	~	~
Nanosecond granularity 64b timestamping	~	•	EVB, VEPA, Flex10, VNTag	~	~	PLDM, MCTP (SMBus or PCIe), RBT	~	~
Ethernet Routing (packet header rewrite)	~	•	512 MAC addresses	~	~			
Packet Tracing and Packet Sniffing	~	•	NAT Offload	~	~	Boot Facilities		
						iSCSI, FCoE, PXE, UEFI	~	~
Streaming						Secure Boot	~	~
Integrated Traffic Management	~	~						
Advanced QoS support	~	•						

Ordering Information

	T7ASIC	N7ASIC		
Memory	Optional	Optional		
Package Size (0.8mm pitch)	31mm	31mm		
400Gb Typ Power*	19-33W	21-29W		
400Gb WC Power*	22-37W	24-31W		
200Gb Typ Power*	11-22W	11-17W		
200Gb WC Power*	14-26W	17-23W		

^{*} Configuration dependent

Physical & Environmental

- Fully RoHS Compliant
- $\bullet~$ Operating Temp: -40° to 55° C or -40° to 131° F
- Operating Humidity: 5 to 95%

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Applications

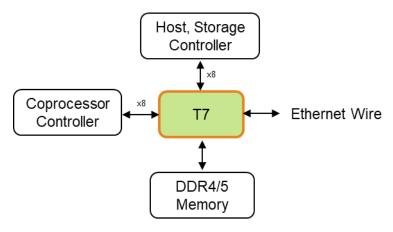


Figure 1 – Generalized Bridge

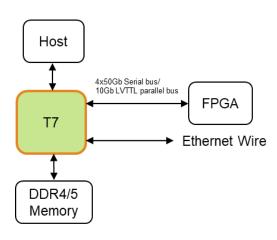


Figure 2 - iNIC Application

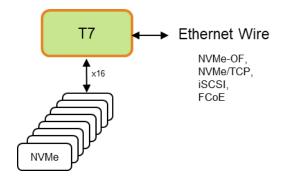


Figure 3 - NVMe-Ethernet Bridge

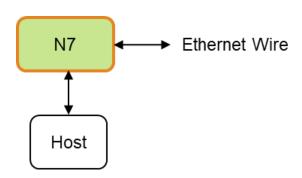


Figure 4 – Legacy Application



Figure 5 - NVMe-NVMe Bridge

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